ABSTRACT

The present invention relates to an event driven digital signal processor 1 comprising: a central arithmetical unit 5, a register 4, a controller 3, an instruction memory 2, and input/output devices. The instruction memory 2 is arranged to include time performance constraints and events. An event control unit 6 is arranged to recognize an event and to control processing to be carried out as a consequence of the event while fulfilling the time performance constraints. The controller 3 is arranged to suspend processing of the time performance constraints after initiating operations in the event control unit 6. The controller 3 resumes processing when advised by the event control unit 6

(fig 1)